37. The memory device of claim 35, wherein the means for determining includes means for comparing each of the plurality of read results with one another.

38. The memory device of claim 35, wherein:

a group of the plurality of memory cells are arranged in a row that includes the first cell; and

the means for determining includes means for determining the likelihood by applying each of the plurality of read voltages when a write is performed on the group of memory cells.

39. The memory device of claim 35, wherein:

a group of the plurality of memory cells are arranged in a row that includes the first cell; and

the means for determining includes means for determining the likelihood by applying each of the plurality of read voltages when a read is performed on the group of memory cells.

40. The memory device of claim 35, wherein the terminal of the first cell is a control gate terminal of the first cell.

41. A method for determining a degradation of a memory device, the method comprising the steps of:

applying a first voltage to a memory cell within the memory device to generate a first read value of the memory cell;

applying a second voltage that is different from the first voltage to the memory cell within the memory device to generate a second read value of the memory cell; and

comparing the first read value to the second read value.

42. The method of claim 41, the method being further for correcting the degradation of the memory device, the method further comprising the step of rewriting a previously stored value into the memory cell when the step of comparing determines that the memory cell has degraded.

43. The method of claim 42, wherein the memory cell is within a row of memory cells within the memory device, the method further comprising the step of rewriting a previously stored value into each of the memory cells within the row.